AMENDMENTS TO THE CLAIMS:

       This listing of claims will replace all prior versions
and listings of claims in the application:

LISTING OF THE CLAIMS:

1.     (Currently amended)   A nonvolatile memory apparatus
comprising a nonvolatile memory and a controller,

       wherein said nonvolatile memory has <u>a first buffer
memory, a second buffer memory, and </u>a plurality of
nonvolatile memory cells each ~~capable of~~ <u>for </u>storing
information of n bits (n: integer of 2 or larger), and ~~can~~
perform<u>s</u> a first reading operation of outputting information
read from ~~said~~ <u>a</u> nonvolatile memory cell as information of m
bits (m: integer smaller than n) and a second reading
operation of outputting information read from said
nonvolatile memory cell as information of n bits,

       <u>wherein in said first reading operation, said
information read from said nonvolatile memory cell is stored
to said first buffer memory without storing to said second
buffer memory,</u>

       <u>wherein in said second reading operation, said
information read from said nonvolatile memory cell is stored</u>

to said second buffer memory, and then is stored to said

first buffer memory, and

    wherein said controller performs the first reading

operation to read first information from said nonvolatile

memory and performs the second reading operation to read

second information from said nonvolatile memory.


2.    (Original)   The nonvolatile memory apparatus according

to claim 1, wherein said first information is validity

management information indicative of validity of a storage

area of said second information.


3.    (Currently amended)   The nonvolatile memory apparatus

according to claim 2, wherein when the nonvolatile memory is

operated according to an instruction from the controller,

said controller checks validity of a storage area of said

second information based on ~~the basis of~~ the validity

management information read from the nonvolatile memory by

performing the first reading operation and, when it is

determined that the storage area is valid, performs the

second reading operation to read the second information from

the nonvolatile memory.

4.    (Currently amended)   The nonvolatile memory apparatus
according to claim 3, wherein said controller checks
validity of a storage area of said second information based
on the basis of validity management information read from
the nonvolatile memory by performing the first reading
operation, when it is determined that the storage area is
invalid, checks validity of the storage area of said second
information based on the basis of the validity management
information read from the nonvolatile memory by performing
the first reading operation on an alternative area of the
storage area of said second information and, when the
storage area is valid, performs the second reading operation
to read the second information from the alternative area.

5.    (Currently amended)   The nonvolatile memory apparatus
according to claim 1,
        wherein said nonvolatile memory cell has a threshold
voltage included in one of four or more threshold voltage
distributions according to information to be stored, and
        wherein at the time of storing said first information
into said nonvolatile memory cell, said nonvolatile memory
uses a predetermined voltage between said threshold voltage
distributions as a boundary, sets, as the threshold voltage
of the nonvolatile memory, any of threshold voltage

distributions of voltages higher than said predetermined

voltage or threshold voltage distributions of voltages lower

than said predetermined voltage, and compares said

predetermined voltage with the threshold voltage of [[a]]

said nonvolatile memory cell in said first reading

operation, thereby reading m-bit information.


6.    (Currently amended)  The nonvolatile memory apparatus

according to claim 5, wherein the threshold voltage of [[a]]

said nonvolatile memory cell in which said first information

is stored is a voltage selected from a voltage in an upper-

limit threshold voltage distribution and a voltage in a

lower-limit threshold voltage distribution.


7.    (Currently amended)  The nonvolatile memory apparatus

according to claim 1,

        wherein said controller can output second information

read from the nonvolatile memory by said second reading

operation to the outside, and can supply said second

information input from the outside to the nonvolatile

memory, and

        wherein said ~~nonvolatile memory has a~~ second buffer

memory ~~buffer which~~ can temporarily store second information

read by said second reading operation before the second

information is supplied to said controller and can
temporarily store second information supplied from said
controller before said second information is stored into
said nonvolatile memory cell.

8.    (Currently amended)  The nonvolatile memory apparatus
according to claim 7, wherein said nonvolatile memory
outputs first information by bypassing said second buffer
memory ~~buffer~~ at the time of reading first information by
said first reading operation.

9.    (Original)  The nonvolatile memory apparatus according
to claim 8, wherein said first information includes validity
management information indicative of validity of a storage
area of said second information.

10.   (Currently amended)  The nonvolatile memory apparatus
according to claim 9, wherein when the nonvolatile memory is
operated according to an instruction from the controller,
said controller checks validity of a storage area of said
second information based on ~~the basis of~~ validity management
information read from the nonvolatile memory by performing
the first reading operation and, when it is determined that

7

the storage area is valid, writes the second information of said <u>second buffer</u> memory ~~buffer~~ into a memory cell.

11.   (Currently amended)  The nonvolatile memory apparatus according to claim 10, wherein said controller checks validity of a storage area of said second information <u>based on</u> ~~the basis of~~ validity management information read from the nonvolatile memory by performing the first reading operation, when it is determined that the storage area is invalid, checks validity of the storage area of said second information <u>based on</u> ~~the basis of~~ validity management information read from the nonvolatile memory by performing the first reading operation on an alternative area of the storage area of said second information and, when the storage area is valid, writes the second information in ~~the~~ <u>said second buffer</u> memory ~~buffer~~ into a memory cell in the alternative area.

12.   (Original)  The nonvolatile memory apparatus according to claim 7, wherein said controller has a controller buffer for temporarily holding second information supplied from the outside and temporarily holding second information read from the nonvolatile memory and supplied.

13.   (Currently amended)   The nonvolatile memory apparatus
according to claim 12, wherein said controller supplies data
from the controller buffer to ~~the~~ <u>said second buffer</u> memory
~~buffer~~, after that, stores the data in ~~the~~ <u>said second</u>
<u>buffer</u> memory ~~buffer~~ to a nonvolatile memory cell and, in
parallel with the storing operation, can input another data
from the outside into the controller buffer.


14.   (Currently amended)   A nonvolatile memory apparatus
comprising a nonvolatile memory and a controller,

wherein said nonvolatile memory has <u>a first buffer</u>
<u>memory, a second buffer memory, and</u> a plurality of
nonvolatile memory cells each ~~of which can be set in an~~ <u>for</u>
<u>storing</u> information ~~storing state included~~ in one of four or
more information storing states, and ~~can~~ performs<u>_</u> a first
reading operation of outputting information read from
[said]<u>a</u> nonvolatile memory cell which is set in said
information storing state as information of m bits (m:
integer of 1 or larger) and a second reading operation of
outputting information read from said nonvolatile memory
cell which is set in said information storing state as
information of n bits (n: integer larger than m),

<u>wherein said first buffer memory is adapted to store</u>
<u>information read from said nonvolatile memory cell in</u>

performing both of said first reading operation and said

second reading operation,

wherein said second buffer memory is adapted to store

information read from said nonvolatile memory cell in

performing said second reading operation, but not store

information read from said nonvolatile memory cell in

performing said first reading operation, and

wherein said controller performs the first reading

operation to read first information from said nonvolatile

memory and performs the second reading operation to read

second information from said nonvolatile memory.


15.    (Original)  The nonvolatile memory apparatus according

to claim 14, wherein an information storing state included

in one of said four or more information storing states is a

threshold voltage state included in one of four or more

threshold voltage distributions of a nonvolatile memory

cell.


16.    (Original)  The nonvolatile memory apparatus according

to claim 15, wherein at the time of storing said first

information into said nonvolatile memory cell, said

nonvolatile memory sets, as a threshold voltage of the

nonvolatile memory cell, a voltage selected from a voltage

in said threshold voltage distribution of the upper limit
and a voltage in said threshold voltage distribution of the
lower limit.

17.   (Currently amended)   The nonvolatile memory apparatus
according to claim 16,

wherein said ~~nonvolatile memory has a~~ second buffer
memory ~~buffer which can~~ holds second information read as n-
bit information from each of a plurality of nonvolatile
memory cells by said second reading operation, suppli_es_[y]
the second information to the controller, holds second
information supplied from said controller, and sets one
nonvolatile memory cell every n bits, at a threshold voltage
included in one of four threshold voltage distributions, and

wherein the first information read as m-bit information
from each of the plurality of nonvolatile memory cells by
said first reading operation is output to said controller
while bypassing said second buffer memory ~~buffer~~.